

Senior Design Engineer

Primary Responsibility:

- Takes a leading role in the development of complex analog circuits and systems needed for completion of the next generation of designs.
- Development of schematic, layout generation, verification, and lab evaluation.
- Provides technical leadership and mentoring to the junior design engineers.
- Architects and designs highly complex circuit and system functions
- Candidate would be encouraged and at times expected to come up with new approaches and architectures. Publishing good technical articles in quality journals and conferences will be expected.
- Responsible for on time delivery and quality of analog blocks
- Regularly interacts with senior management. Interactions normally involve communicating, updating or informing regarding technical or personnel issues and may extend to customer meetings.

Education/Experience:

- Bachelor's degree (from IIT, NIT) Master's degree (from IISc, IIT).
- 3-5 years of experience in the semiconductor analog design.
- Experience in the analog design of phy chips for high-speed / high performance communication applications is a plus.
- Understand the design of analog blocks used in phy chips for high-speed communications: equalizers, PLLs, CDRs, high speed drivers, FIR drivers, MUX and Demux, ADC, DAC.
- Familiarity with the latest Analog design tools and techniques
- Experience with device, passive, and behavior models is a plus.
- Experience with deep sub-micron technologies is a plus.
- Past history of being named as an inventor on circuit/architectural patents is a plus.
- An architect and leader on either the whole chip or complex big analog blocks, for multiple chips, highly preferred.

Other Details:

- Be able to work in a start-up environment
- Detail oriented
- Strong written and verbal communication skills
- Highly developed interpersonal skills; builds strong relationships with customers and internal resources
- Location will be Kharagpur (IIT Campus)