

Job title: Synthesis/STA Lead

Job Description:

Need to lead/execute the logic synthesis & Static Timing Analysis (STA) for multi-million gate digital blocks for customers in Deep Sub-micron/Ultra-Deep Sub-micron technology nodes independently. Work will include constraints definition, constraints optimization, timing closure, automation etc. Timing closure challenges, design closure challenges will be abundant along with the opportunity to work with industry experts on the state-of-the-art processes, tools and flows.

Place of work:

Indore (M.P) (Based on project needs, onsite at Bangalore for short durations might be needed)

Basic Qualifications needed:

- An engineering degree (Bachelor/Masters) in Electrical & Electronics/ Electronics & Communication/ Instrumentation
- 4+ years of hands-on experience in Logic synthesis/STA. Experience in both
- Synthesis & STA preferred.
- Independent contributor with good expertise in
 1. Logic Synthesis
 2. Timing Constraints
 3. Static Timing Analysis
 4. Timing Closure
- Exposure to industry standard tools (Synopsys, Cadence)
- Good communication & problem solving skills

Additional Preferred Qualifications:

- Experience in leading chip level synthesis/STA
- Working experience in scripting languages such as PERL, TCL etc.
- Familiarity with make/gmake
- Knowledge of Ultra-Deep Submicron (UDSM) issues in digital backend
- Expertise in formal verification.
- Self-driven in learning and execution, Willingness to work hard and strong teaming skills.

Compensation & Benefits:

- Attractive package will be offered as per industry practices.